[**CS 385 - Computer Architecture**](https://www.cs.ccsu.edu/%7Emarkov/ccsu_courses/385Syllabus.html)

**General**

The X-ed out part in the CPU picture is the thing that interprets the funct field in a standard mips cpu: we’re not using that in our simplified CPU design

Original behavioral model of MIPS - single cycle implementation, R-types and addi:

<https://www.cs.ccsu.edu/~markov/ccsu_courses/mips-r-type_addi.vl>

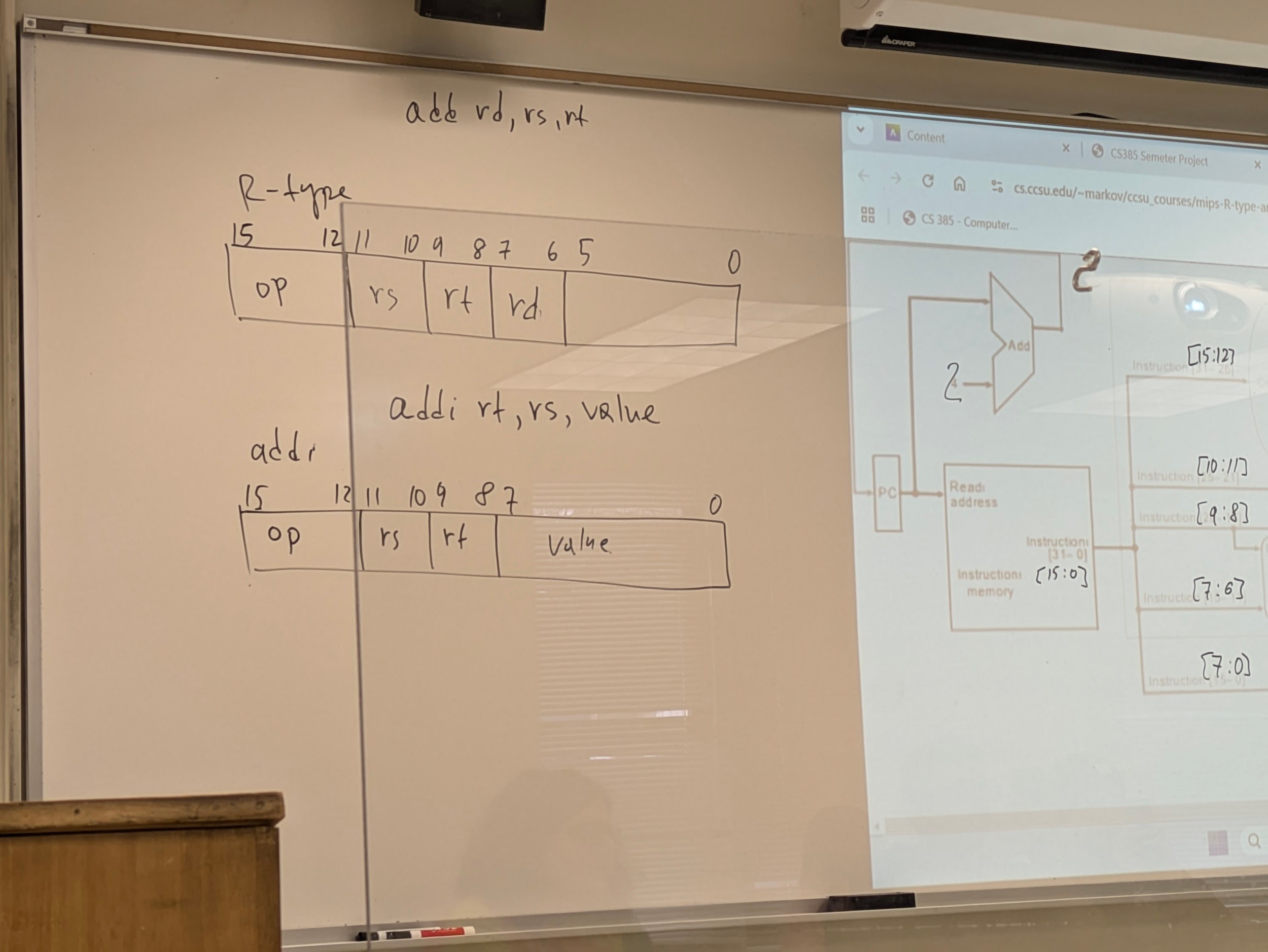
Make sure to do everything at behavioral level first to make sure it works; if you go right into gate level, debugging becomes impossible fast.

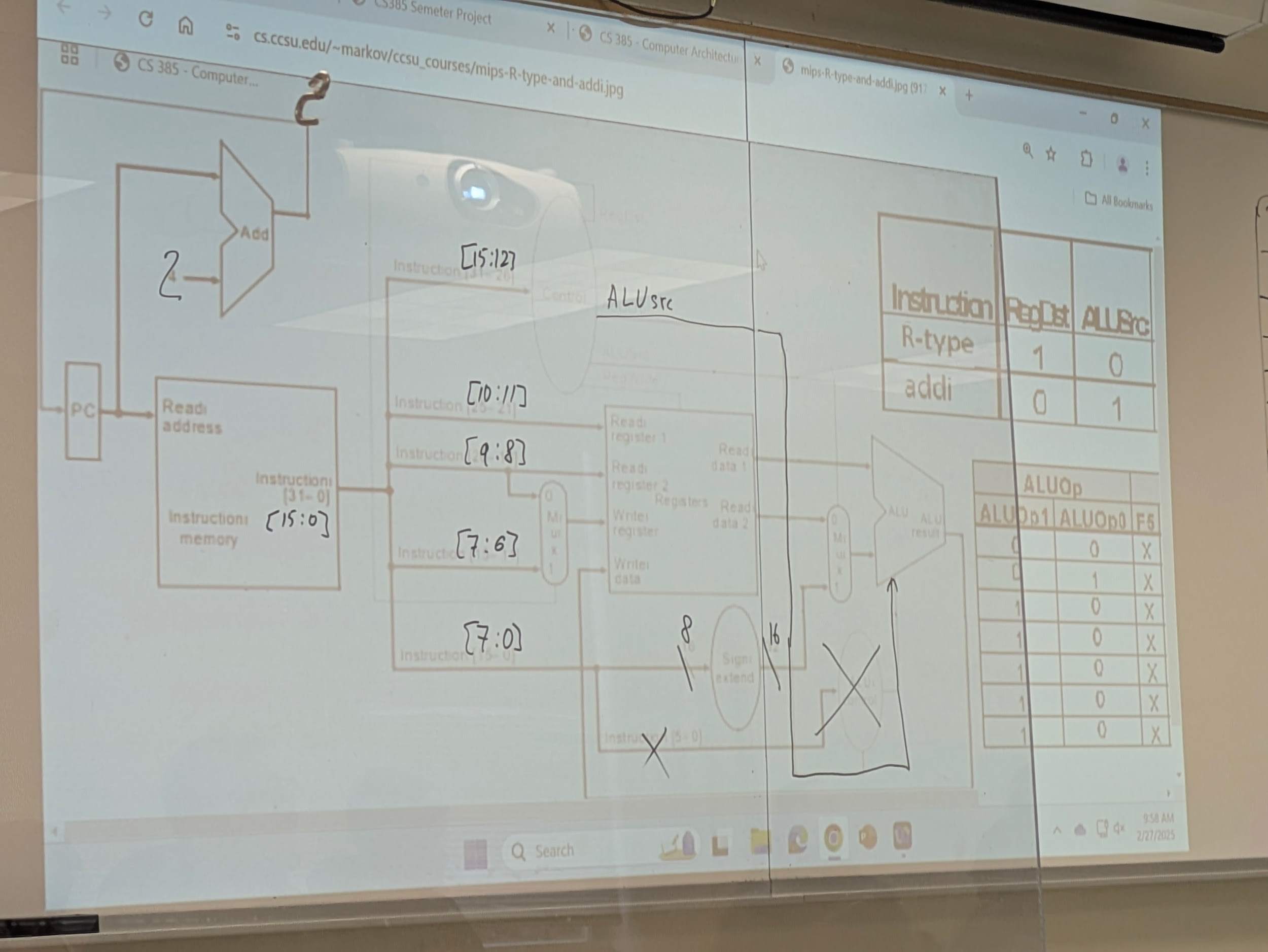
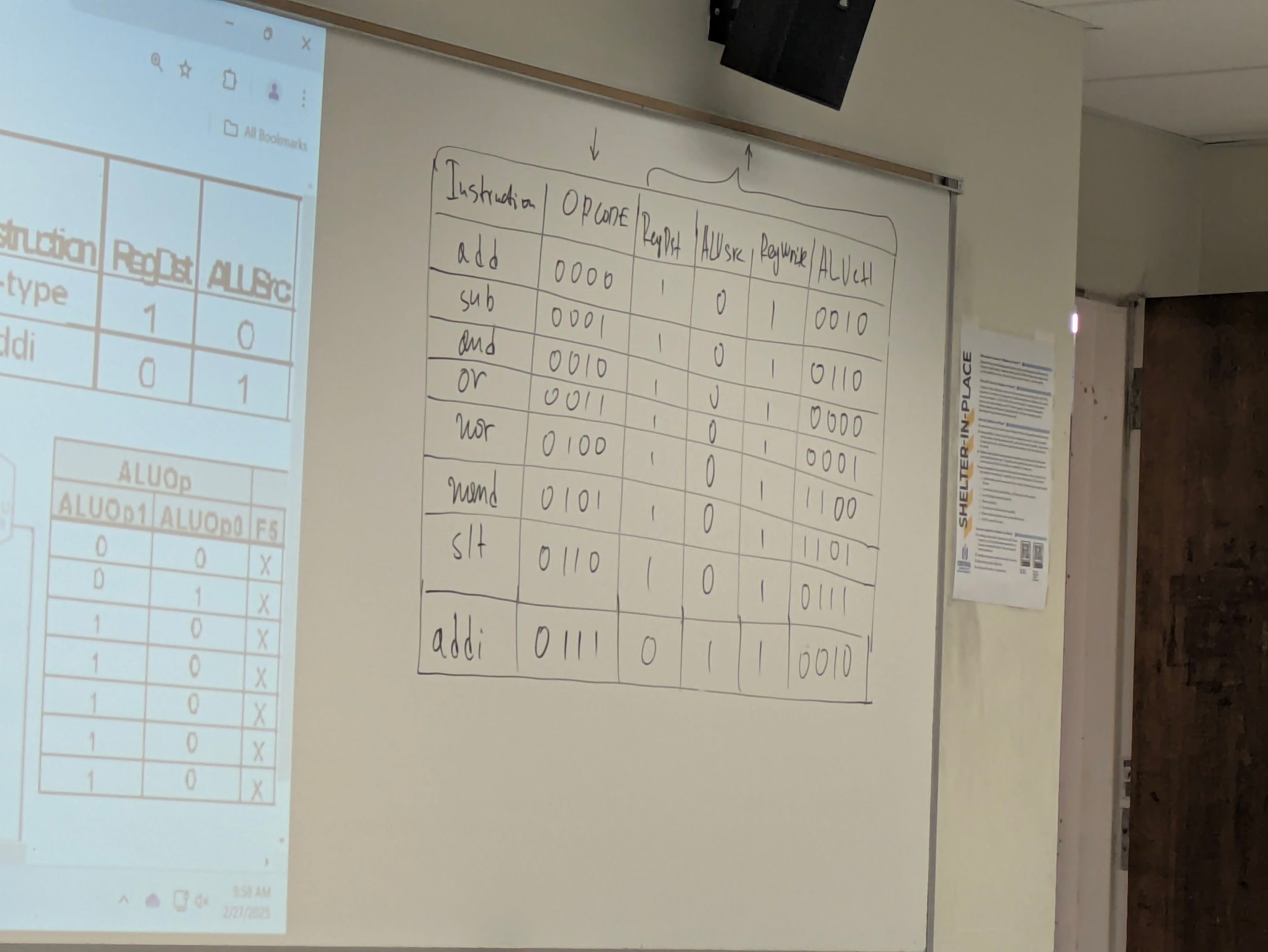
**Key idea: fail fast**

If you make a mistake, you want it to become apparent as soon as possible to avoid having to sift through lots of complexity to fix i

To be implemented at gate level:

ALU, 2 bit 2:1 multiplexers, 16-bit 2:1 multiplexer (made of 16 2:1s)





**Lecture Material**

**Questions**

**TODO:**